APPENDIX A

Figure 19 is a schematic diagram illustrating an example of an input stage of an offsetable differential receiver in accordance with an embodiment of the invention. A differential input signal is coupled to an input 1901 at a gate of a first input transistor 1903 and to an input 1902 at a gate of a second input transistor 1904. A source of the first input transistor 1903 and a source of the second input transistor 1904 are coupled to a first terminal 1911~~9~~ of current source 1912~~0~~. A second terminal 19~~2~~13 of current source 1912~~0~~ is coupled to ground.